Reg. No. : | | | | | | | | | | | | |

Question Paper Code : X67557

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester
Electronics and Communication Engineering
EC1201 – DIGITAL ELECTRONICS
(Regulations 2008)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Convert 41.6875_{10} to binary.
2. Construct AND gate using NAND gates.
3. Draw the inverter logic circuit using n-channel MOS devices.
4. What is totem-pole output ?
5. Draw the logic circuit for the expression $F = \bar{x}\,\bar{y}\,z + \bar{x}\,y\,z + x\,\bar{y}$
6. Define modulus of a counter.
7. Draw the logic diagram of D flipflop using NAND gates.
8. How does JK filip flop differ from an S – R flip flop in its basic operation ?
9. Distinguish between EAPROM and EEPROM.
10. Write about FPGA.

PART – B **(5×16=80 Marks)**

11. a) i) Design the circuit for one bit comparator. **(8)**

    ii) Design a full adder circuit using NAND gates only. **(8)**

    (OR)

    b) i) Write a detailed technical note on the Hardware Description Language. **(8)**

    ii) What is Karnaugh Map ? A truth table has output 0 for input ABCD = 0000, 0010, 1100, 1101, 1110, 1111, 0101, 0111. Simplify using Karnaugh Map and draw the simplified circuit. **(8)**

12. a) Explain the construction and operation of DTL and TTL NAND gate. Also mention the characteristics of DTL and TTL families. **(16)**

(OR)

b) i) Explain CMOS NAND and NOR gate operation. **(8)**

ii) Explain the working of tristate logic. **(8)**

13. a) i) Design and implement an 8 × 1 multiplexer using suitable gates. **(8)**

ii) Design a 3 bit parity generator and checker circuit. **(8)**

(OR)

b) i) Design and implement full subtractor using suitable gates. **(8)**

ii) Design the logic diagram of magnitude comparator to compare two binary variables A and B accompanied by 3 bits each. **(8)**

14. a) i) Design a synchronous decade counter to count in the following sequence. 1, 0, 2, 3, 4, 8, 7, 6, 5. **(8)**

ii) What is sequential circuit ? Explain S-R and J K flip flop. **(8)**

(OR)

b) i) Draw and explain 4-bit synchronous Up/Down counter. **(8)**

ii) Design a serial 2's complementer with a shaft register and a flip-flop. The binary number is shifter out from one side and its 2's complement shifted into the other side of the shift register. **(8)**

15. a) i) Draw the circuit of a BJT RAM cell and explain its operation. **(8)**

ii) Give the classification of memory and explain the block diagram of ROM. **(8)**

(OR)

b) Along with neat diagrams write a detailed technical note on the following

i) MOSFET RAM cell. **(8)**

ii) FPGA. **(8)**

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